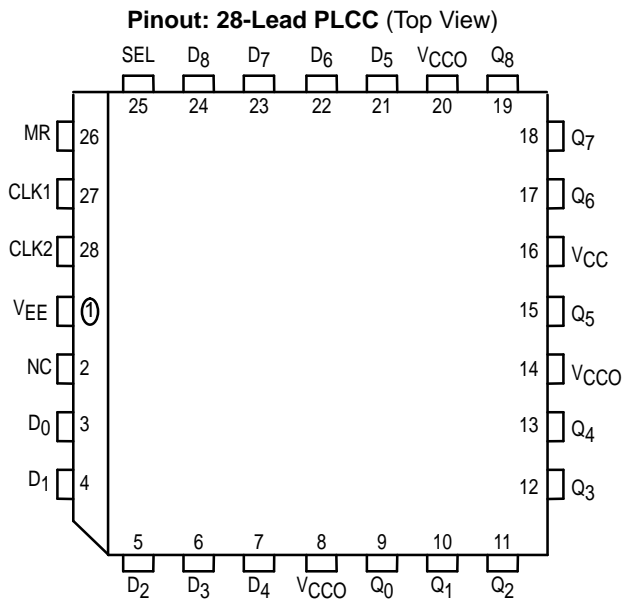


9-Bit Hold Register

The MC10E100E143 is a 9-bit holding register, designed with byte-parity applications in mind. The E143 holds current data or loads new data, with the nine inputs D0 – D8 accepting parallel input data.

- 700MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

The SEL (Select) input pin is used to switch between the two modes of operation — HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

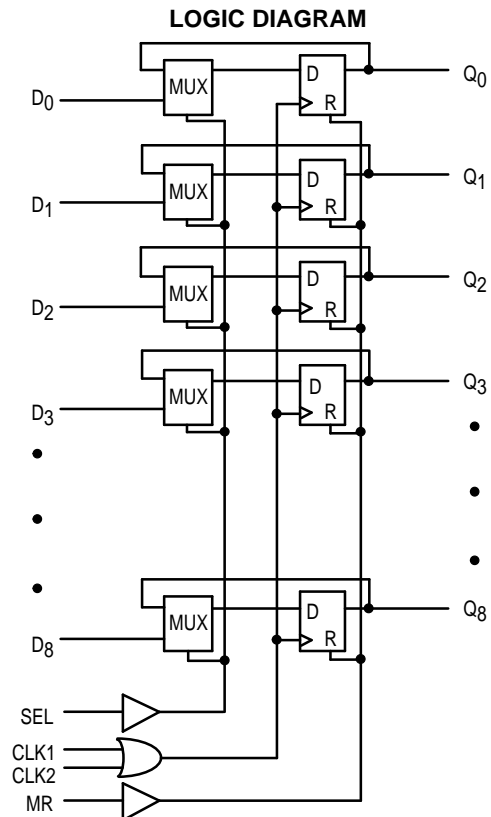
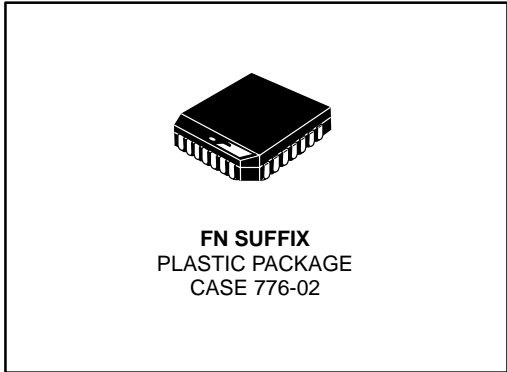


PIN NAMES

Pin	Function
D ₀ – D ₈	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q ₀ – Q ₈	Data Outputs
NC	No Connection

FUNCTIONS

SEL	Mode
L	Load
H	Hold



DC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = V_{CCO} = \text{GND}$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		120	145		120	145		120	145		
	100E		120	145		120	145		138	165		

AC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = V_{CCO} = \text{GND}$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{MAX}	Max. Toggle Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output Clk MR	600	800	1000	600	800	1000	600	800	1000	ps	
t_s	Setup Time D SEL	50	-100		50	-100		50	-100		ps	
		300	150		300	150		300	150			
t_h	Hold Time D SEL	300	100		300	100		300	100		ps	
		75	-150		75	-150		75	-150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width Clk, MR	400			400			400			ps	
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r t_f	Rise/Fall Times 20 - 80%	300	525	800	300	525	800	300	525	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

OUTLINE DIMENSIONS


FN SUFFIX
 PLASTIC PLCC PACKAGE
 CASE 776-02
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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